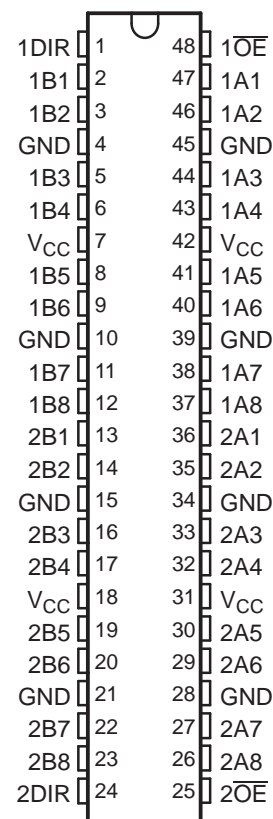


## FEATURES

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Distributed  $V_{CC}$  and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

SN54LVTH16245A . . . WD PACKAGE  
SN74LVTH16245A . . . DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## DESCRIPTION/ORDERING INFORMATION

The 'LVTH16245A devices are 16-bit (dual-octal) noninverting 3-state transceivers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

The devices are designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input and the output-enable ( $\overline{OE}$ ) input activate either the B-port outputs or the A-port outputs or place both output ports into the high-impedance mode. The device transmits data from the A bus to the B bus when the B-port outputs are activated, and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports is always active and must have a logic HIGH or LOW level applied to prevent excess  $I_{CC}$  and  $I_{CCZ}$ .

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When  $V_{CC}$  is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

# SN54LVTH16245A, SN74LVTH16245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

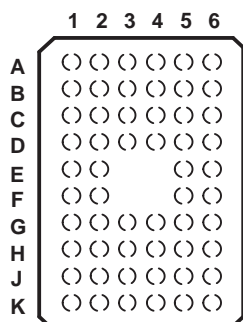
SCBS143R – MAY 1992 – REVISED NOVEMBER 2006

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	FBGA – GRD	Reel of 1000	SN74LVTH16245AGRDR	LL245A
	FBGA – ZRD (Pb-free)		SN74LVTH16245AZRDR	
	SSOP – DL	Tube of 25	74LVTH16245ADL	LVTH16245A
			74LVTH16245ADLG4	
		Reel of 1000	74LVTH16245ADLR	
			74LVTH16245ADLRG4	
	TSSOP – DGG	Reel of 2000	SN74LVTH16245ADGGR	LVTH16245A
			74LVTH16245ADGGRE4	
			74LVTH16245ADGGRG4	
	TVSOP – DGV	Reel of 2000	SN74LVTH16245ADGVR	LL245A
74LVTH16245ADGVRE4				
-55°C to 125°C	VFBGA – GQL	Reel of 1000	SN74LVTH16245AGQLR	LL245A
	VFBGA – ZQL (Pb-free)		74LVTH16245AZQLR	
	CFP – WD	Tube	SNJ54LVTH16245AWD	SNJ54LVTH16245AWD

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

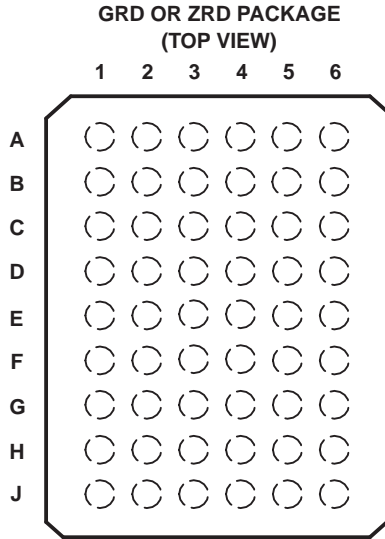
### GQL OR ZQL PACKAGE (TOP VIEW)



### TERMINAL ASSIGNMENTS<sup>(1)</sup> (56-Ball GQL/ZQL Package)

	1	2	3	4	5	6
<b>A</b>	1DIR	NC	NC	NC	NC	1 $\overline{OE}$
<b>B</b>	1B2	1B1	GND	GND	1A1	1A2
<b>C</b>	1B4	1B3	V <sub>CC</sub>	V <sub>CC</sub>	1A3	1A4
<b>D</b>	1B6	1B5	GND	GND	1A5	1A6
<b>E</b>	1B8	1B7			1A7	1A8
<b>F</b>	2B1	2B2			2A2	2A1
<b>G</b>	2B3	2B4	GND	GND	2A4	2A3
<b>H</b>	2B5	2B6	V <sub>CC</sub>	V <sub>CC</sub>	2A6	2A5
<b>J</b>	2B7	2B8	GND	GND	2A8	2A7
<b>K</b>	2DIR	NC	NC	NC	NC	2 $\overline{OE}$

(1) NC – No internal connection



**TERMINAL ASSIGNMENTS<sup>(1)</sup>**  
**(54-Ball GRD/ZRD Package)**

	1	2	3	4	5	6
<b>A</b>	1B1	NC	1DIR	1 $\overline{OE}$	NC	1A1
<b>B</b>	1B3	1B2	NC	NC	1A2	1A3
<b>C</b>	1B5	1B4	V <sub>CC</sub>	V <sub>CC</sub>	1A4	1A5
<b>D</b>	1B7	1B6	GND	GND	1A6	1A7
<b>E</b>	2B1	1B8	GND	GND	1A8	2A1
<b>F</b>	2B3	2B2	GND	GND	2A2	2A3
<b>G</b>	2B5	2B4	V <sub>CC</sub>	V <sub>CC</sub>	2A4	2A5
<b>H</b>	2B7	2B6	NC	NC	2A6	2A7
<b>J</b>	2B8	NC	2DIR	2 $\overline{OE}$	NC	2A8

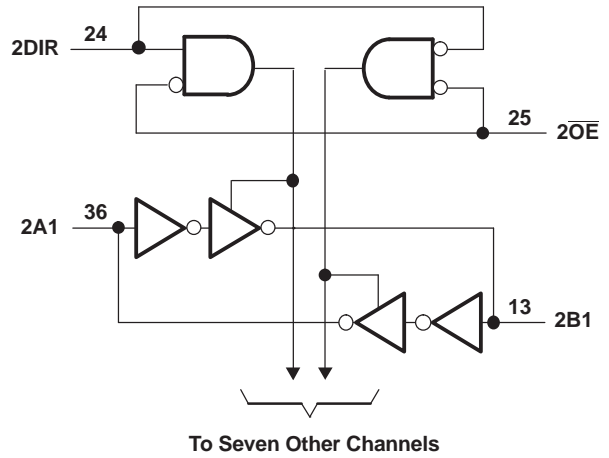
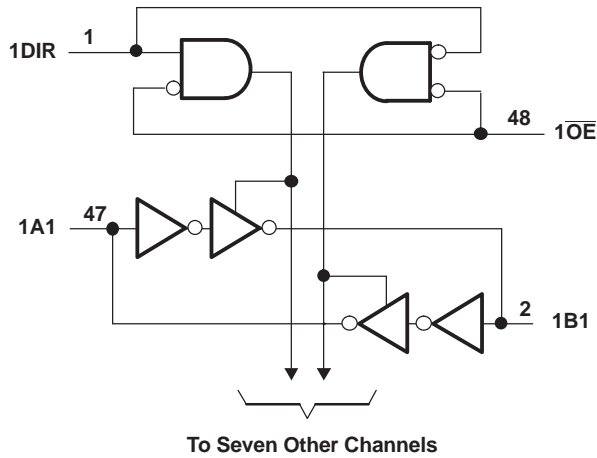
(1) NC – No internal connection

**FUNCTION TABLE<sup>(1)</sup>**  
**(EACH 8-BIT SECTION)**

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A bus
L	H	Hi-Z	Enabled	A data to B bus
H	X	Hi-Z	Hi-Z	Isolation

(1) Input circuits of the data I/Os always are active.

**LOGIC DIAGRAM (POSITIVE LOGIC)**



# SN54LVTH16245A, SN74LVTH16245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143R–MAY 1992–REVISED NOVEMBER 2006

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	4.6	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high state <sup>(2)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_O$	Current into any output in the low state	SN54LVTH16245A	96	mA
		SN74LVTH16245A	128	
$I_O$	Current into any output in the high state <sup>(3)</sup>	SN54LVTH16245A	48	mA
		SN74LVTH16245A	64	
$I_{IK}$	Input clamp current	$V_I < 0$	-50	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>	DGG package	70	°C/W
		DGV package	58	
		DL package	63	
		GQL/ZQL package	42	
		GRD/ZRD package	36	
$T_{stg}$	Storage temperature range	-65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

(3) This current flows only when the output is in the high state and  $V_O > V_{CC}$ .

(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

		SN54LVTH16245A		SN74LVTH16245A		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		-24		-32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate		10		10	ns/V
	Outputs enabled		10		10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	-55	125	-40	85	°C

(1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**Electrical Characteristics**

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN54LVTH16245A			SN74LVTH16245A			UNIT
				MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
$V_{IK}$		$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2			-1.2			V
$V_{OH}$		$V_{CC} = 2.7\text{ V to } 3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC} - 0.2$			$V_{CC} - 0.2$			V
		$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4			2.4			
		$V_{CC} = 3\text{ V}$		2			2			
$V_{OL}$		$V_{CC} = 2.7\text{ V}$		$I_{OL} = 100\text{ }\mu\text{A}$		0.2			0.2	V
				$I_{OL} = 24\text{ mA}$		0.5			0.5	
		$V_{CC} = 3\text{ V}$		$I_{OL} = 16\text{ mA}$		0.4			0.4	
				$I_{OL} = 32\text{ mA}$		0.5			0.5	
				$I_{OL} = 48\text{ mA}$		0.55				
				$I_{OL} = 64\text{ mA}$					0.55	
$I_I$		Control inputs $V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$ $V_{CC} = 0\text{ or } 3.6\text{ V}$ , $V_I = 5.5\text{ V}$		$\pm 1$			$\pm 1$			$\mu\text{A}$
				10			10			
		A or B port <sup>(2)</sup> $V_{CC} = 3.6\text{ V}$		$V_I = 5.5\text{ V}$		20			20	
				$V_I = V_{CC}$		5			5	
$I_{off}$		$V_{CC} = 0$ , $V_I\text{ or } V_O = 0\text{ to } 4.5\text{ V}$					$\pm 100$			$\mu\text{A}$
$I_{I(\text{hold})}$		$V_{CC} = 3\text{ V}$		$V_I = 0.8\text{ V}$		75			75	$\mu\text{A}$
				$V_I = 2\text{ V}$		-75			-75	
		$V_{CC} = 3.6\text{ V}$ , <sup>(3)</sup> $V_I = 0\text{ to } 3.6\text{ V}$					500 -750			
$I_{OZPU}$		$V_{CC} = 0\text{ to } 1.5\text{ V}$ , $V_O = 0.5\text{ V to } 3\text{ V}$ , $OE = \text{don't care}$		$\pm 100$ <sup>(4)</sup>			$\pm 100$			$\mu\text{A}$
$I_{OZPD}$		$V_{CC} = 1.5\text{ V to } 0$ , $V_O = 0.5\text{ V to } 3\text{ V}$ , $OE = \text{don't care}$		$\pm 100$ <sup>(4)</sup>			$\pm 100$			$\mu\text{A}$
$I_{CC}$		$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$		Outputs high		0.19			0.19	mA
				Outputs low		5			5	
				Outputs disabled		0.19			0.19	
$\Delta I_{CC}$ <sup>(5)</sup>		$V_{CC} = 3\text{ V to } 3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$		0.2			0.2			mA
$C_i$		$V_I = 3\text{ V or } 0$		4			4			pF
$C_{io}$		$V_O = 3\text{ V or } 0$		10			10			pF

 (1) All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

 (2) Unused pins at  $V_{CC}\text{ or GND}$ 

(3) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(4) On products compliant to MIL-PRF-38535, this parameter is not production tested.

 (5) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}\text{ or GND}$ .

# SN54LVTH16245A, SN74LVTH16245A 3.3-V ABT 16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

SCBS143R–MAY 1992–REVISED NOVEMBER 2006

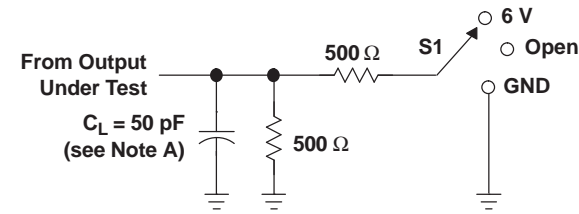
## Switching Characteristics

over recommended operating free-air temperature range,  $C_L = 50$  pF (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16245A				SN74LVTH16245A				UNIT	
			$V_{CC} = 3.3$ V $\pm 0.3$ V		$V_{CC} = 2.7$ V		$V_{CC} = 3.3$ V $\pm 0.3$ V			$V_{CC} = 2.7$ V		
			MIN	MAX	MIN	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN		MAX
$t_{PLH}$	A or B	B or A	0.5	4.5	4.6		1.5	2.3	3.3	3.7		ns
$t_{PHL}$			0.5	4.4	3.9		1.3	2.1	3.3	3.5		
$t_{PZH}$	$\overline{OE}$	A or B	0.5	6.5	6.6		1.5	2.8	4.5	5.3		ns
$t_{PZL}$			0.5	5.4	6.2		1.6	2.9	4.6	5.2		
$t_{PHZ}$	$\overline{OE}$	A or B	1	6.8	7		2.3	3.7	5.1	5.5		ns
$t_{PLZ}$			1	6.2	6.3		2.2	3.5	5.1	5.4		
$t_{sk(LH)}$								0.5	0.5		ns	
$t_{sk(HL)}$								0.5	0.5			

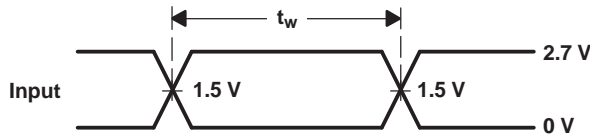
(1) All typical values are at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$ .

PARAMETER MEASUREMENT INFORMATION

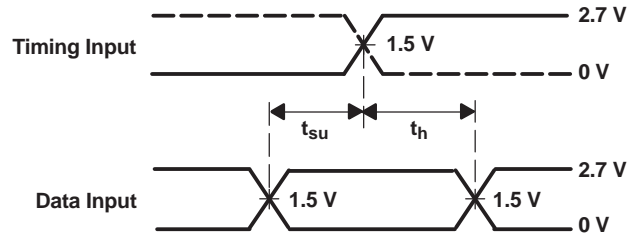


LOAD CIRCUIT

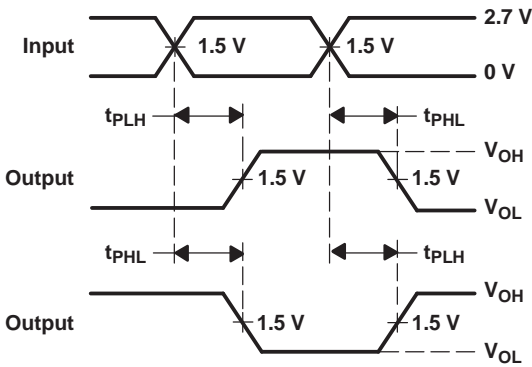
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



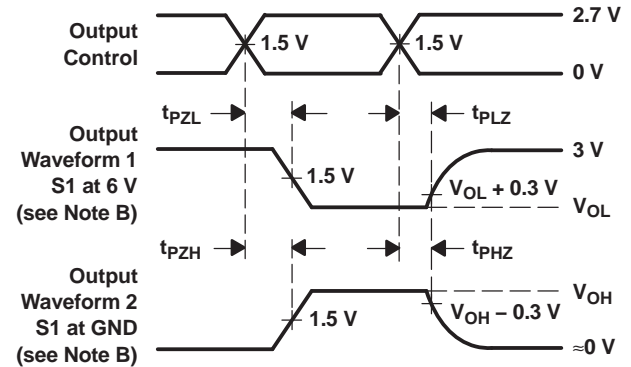
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9668601QXA	ACTIVE	CFP	WD	48	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9668601QX A SNJ54LVTH16245 AWD	<a href="#">Samples</a>
5962-9668601VXA	ACTIVE	CFP	WD	48	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9668601VX A SNV54LVTH16245 AWD	<a href="#">Samples</a>
74LVTH16245ADGGRE4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16245A	<a href="#">Samples</a>
74LVTH16245ADGGRG4	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16245A	<a href="#">Samples</a>
74LVTH16245ADGVRG4	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LL245A	<a href="#">Samples</a>
74LVTH16245ADLG4	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16245A	<a href="#">Samples</a>
74LVTH16245ADLRG4	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16245A	<a href="#">Samples</a>
SN74LVTH16245ADGGR	ACTIVE	TSSOP	DGG	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16245A	<a href="#">Samples</a>
SN74LVTH16245ADGVR	ACTIVE	TVSOP	DGV	48	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LL245A	<a href="#">Samples</a>
SN74LVTH16245ADL	ACTIVE	SSOP	DL	48	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16245A	<a href="#">Samples</a>
SN74LVTH16245ADLR	ACTIVE	SSOP	DL	48	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16245A	<a href="#">Samples</a>
SNJ54LVTH16245AWD	ACTIVE	CFP	WD	48	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-9668601QX A SNJ54LVTH16245 AWD	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.



(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVTH16245A, SN54LVTH16245A-SP, SN74LVTH16245A :**

- Catalog: [SN74LVTH16245A](#), [SN54LVTH16245A](#)
  
- Automotive: [SN74LVTH16245A-Q1](#), [SN74LVTH16245A-Q1](#)
  
- Enhanced Product: [SN74LVTH16245A-EP](#), [SN74LVTH16245A-EP](#)
  
- Military: [SN54LVTH16245A](#)
  
- Space: [SN54LVTH16245A-SP](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16245ADGGR	TSSOP	DGG	48	2000	330.0	24.4	8.6	13.0	1.8	12.0	24.0	Q1
SN74LVTH16245ADGVR	TVSOP	DGV	48	2000	330.0	16.4	7.1	10.2	1.6	12.0	16.0	Q1
SN74LVTH16245ADLR	SSOP	DL	48	1000	330.0	32.4	11.35	16.2	3.1	16.0	32.0	Q1

## TAPE AND REEL BOX DIMENSIONS



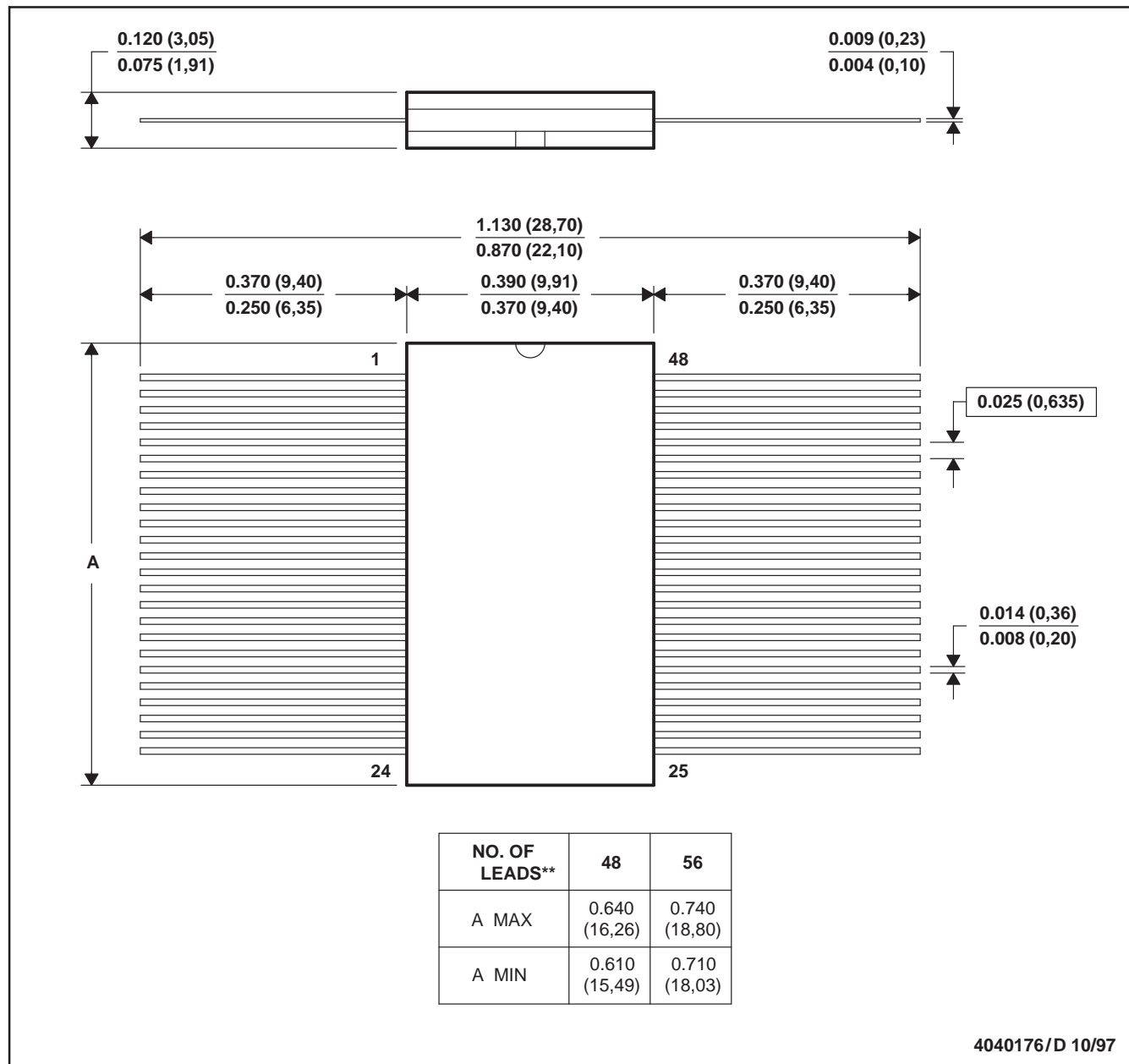
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16245ADGGR	TSSOP	DGG	48	2000	367.0	367.0	45.0
SN74LVTH16245ADGVR	TVSOP	DGV	48	2000	853.0	449.0	35.0
SN74LVTH16245ADLR	SSOP	DL	48	1000	367.0	367.0	55.0

WD (R-GDFP-F\*\*)

CERAMIC DUAL FLATPACK

48 LEADS SHOWN

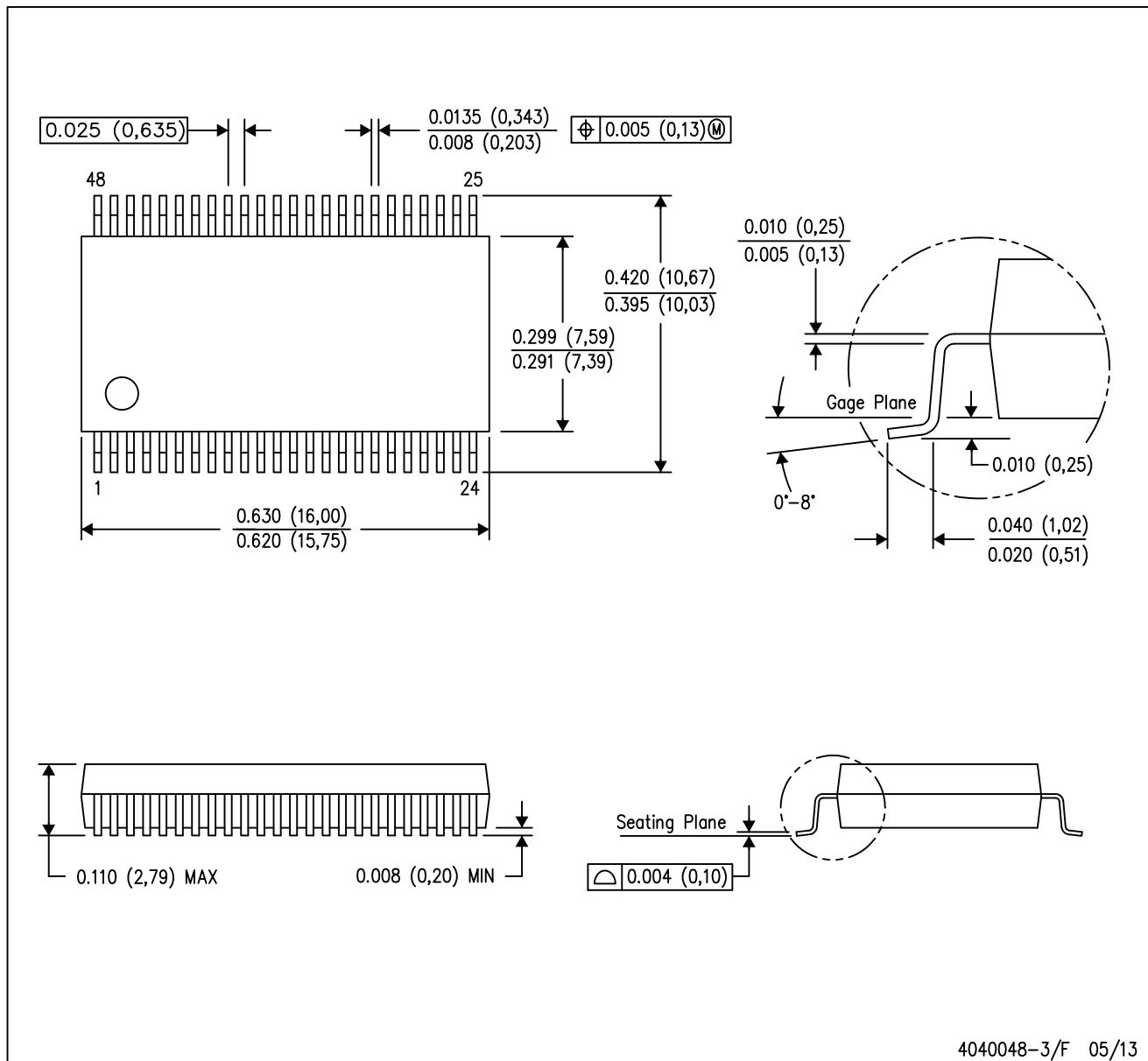


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. This package can be hermetically sealed with a ceramic lid using glass frit.  
 D. Index point is provided on cap for terminal identification only  
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA  
 GDFP1-F56 and JEDEC MO-146AB

# MECHANICAL DATA

DL (R-PDSO-G48)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MO-118

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DGV (R-PDSO-G\*\*)

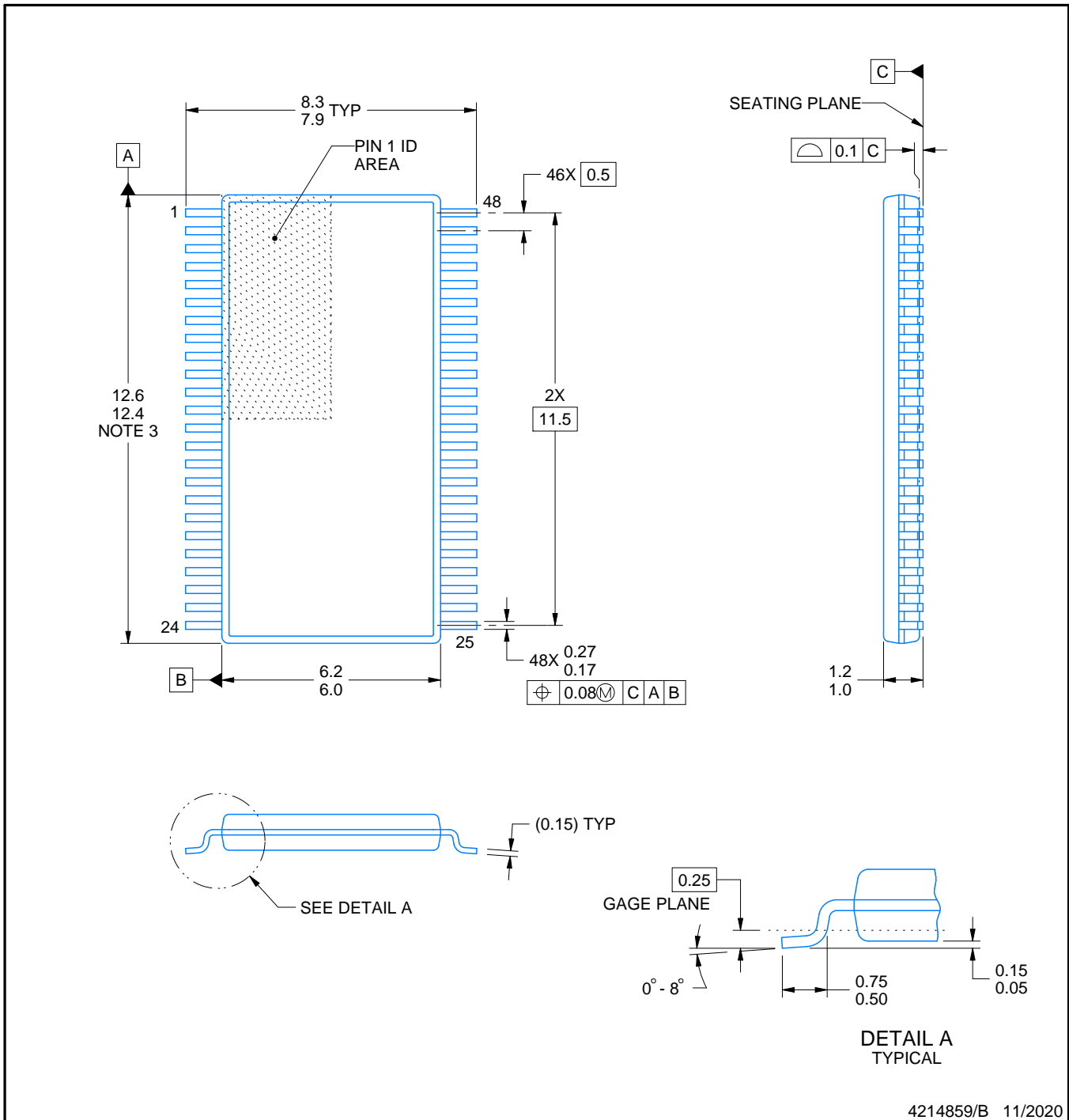
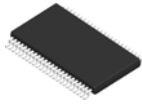
PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

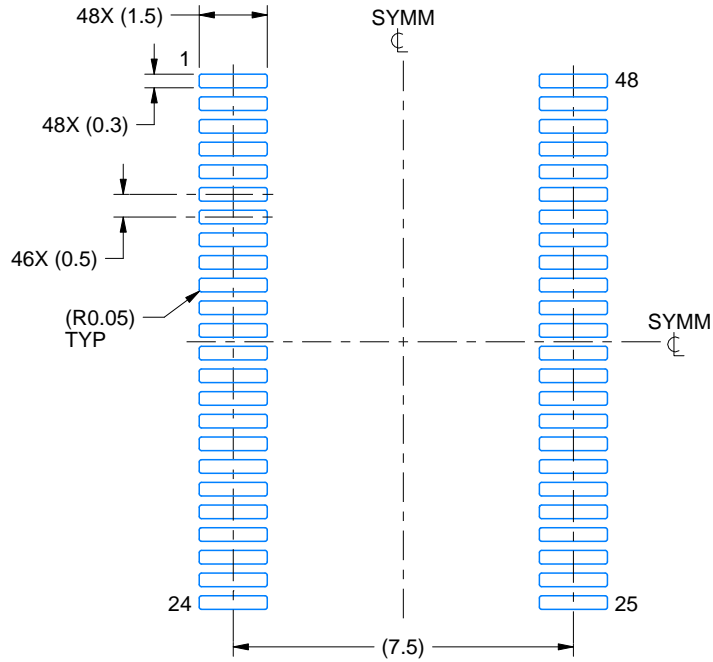


# EXAMPLE BOARD LAYOUT

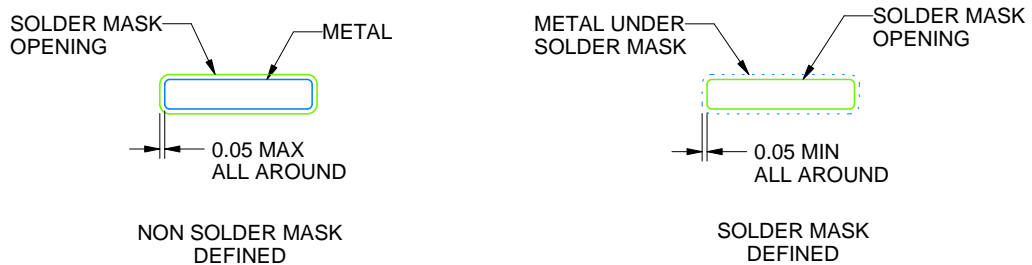
DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

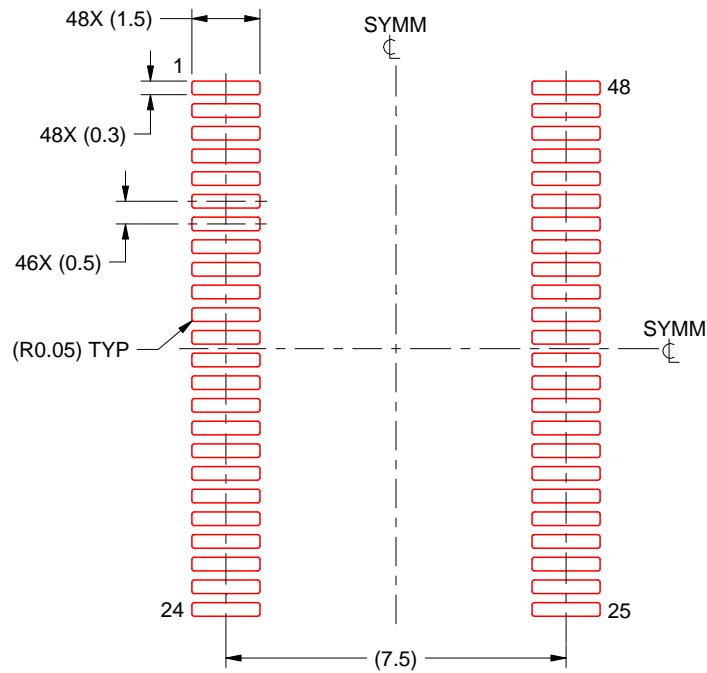
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DGG0048A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4214859/B 11/2020

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
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